



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Akito Hara  
Serial No.: 10/790,875  
Conf. No.: 4718  
Filed: 3/2/2004  
For: SEMICONDUCTOR DEVICE  
AND METHOD OF  
FABRICATING THE SAME  
Art Unit: 2811  
Examiner: Nguyen, Cuong Quang

*I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: MS Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.*

6 April 05   
Date Registration No. 29,367  
Attorney for Applicant(s)

REQUEST FOR ACKNOWLEDGEMENT OF PREVIOUSLY CITED REFERENCE


Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Applicants request acknowledgement of the Makihiro reference cited in an Information Disclosure Statement on June 7, 2004. The Makihiro reference was not acknowledged, apparently through inadvertent error. A copy of the initialed PTO-1449 form and the Makihiro reference is enclosed.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By   
Patrick G. Burns  
Registration No. 29,367

April 6, 2005

300 South Wacker Drive  
Suite 2500  
Chicago, Illinois 60606  
Telephone: 312.360.0080  
Facsimile: 312.360.9315

Customer No. 24978

Form PTO-1449  
(Rev. 8-88)U.S. Department of Commerce  
Patent & Trademark Office

Attorney Docket No.: 1117.69877

Serial No.: 10/790,875

Applicant: Akito Hara

INFORMATION DISCLOSURE CITATION  
(Use several sheets if necessary)

Filing Date: 3/2/2004

Group: 2811

## U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
Ch	2002/0031876	Mar. 14, 2002	Hara et al.	438	166	8-22-01

## FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
Ch	10-173192	Jun. 26, 1998	Japan			Abs. only	
Ch	2002-033481	Jan. 31, 2002	Japan			Abs. only	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Makihira et al.; Double-Gate Poly-Si Thin-Film Transistors Fabricated Using Self-Aligned Technology; Am-LCD '01; Digest of Technical Papers; July 11-13, 2001

Examiner

Date Considered

\*Examiner:

Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.